

PRELIMINARY AMENDMENT

Page 25

Serial Number: 10/177213

Filing Date: June 21, 2002

Title: WRITE ONCE READ ONLY MEMORY WITH LARGE WORK FUNCTION FLOATING GATES

REMARKS

The Applicant respectfully requests that the amendment described herein be entered into the record prior to examination and consideration of the above-identified application. The Examiner is invited to contact Applicant's Representatives at the below-listed telephone number if there are any questions regarding this amendment or if prosecution of this application may be assisted thereby.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
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(612) 373-6960

Date 9-22-03

By Marvin L. Beekman
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of September, 2003.

Amy Moriarty
Name

Amy Moriarty
Signature



2818

PATENT

JP

10/028001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Tu-Tu V. Ho

Serial No.: 10/028001

Group Art Unit: 2818

Filed: December 20, 2001

Docket: 1303.035US1

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL
DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Noted, TH, 11/14/03

Applicants would like to bring to the Examiner's attention the following related co-pending application(s) in the above-identified patent application:

| <u>Serial No.</u> | <u>Filing Date</u> | <u>Attorney Docket</u> | <u>Title</u> |
|-------------------|--------------------|------------------------|--|
| 09/945395 | August 30, 2001 | 1303.019US1 | DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS |
| 09/943134 | August 30, 2001 | 1303.020US1 | PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS |
| 09/945512 | August 30, 2001 | 1303.027US1 | IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS |
| 09/945554 | August 30, 2001 | 1303.028US1 | SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS |
| 10/081818 | February 20, 2002 | 1303.045US1 | ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS |

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 10/028001

Filing Date: December 20, 2001

Title: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

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Dkt: 1303.035US1

10/177096 June 21,
2002

1303.063US1

GRADED COMPOSITION METAL
OXIDE TUNNEL BARRIER INTERPOLY
INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

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Name

Amy Moriarty

Signature

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